Institute of Electrical and Electronics Engineers
(IEEE) Hyderabad Section
Joint Chapter of Circuits and Systems & Electron Devices Societies (CAS/EDS)

AMS Semiconductors &
Anurag Group of Institutions
Presents Workshop on

Analog Integrated Circuit Design (Concept to Reality)

CHIEF PATRON
Dr. P. Rajeshwar Reddy
Chairman, AGI
Mrs.S. Neelima
Secretary/Correspondent

PATRON
Dr. K.S.Rao
Director, AGI
Dr.Vishnumurthy
Dy.Director, AGI

CONVENER
Dr.S. Sateesh Kumaran
Head of the department, ECE.

ORGANIZING COMMITTEE:
Dr. Mohammed Arifuddin Sohel,
Chair, IEEE CAS/EDS joint Chapter
9885 407 094, arif.sohel@ieee.org

Dr. A. G. Krishna Kanth,
Vice Chair, IEEE CAS/EDS Chapter,
9989644633, kk.avalur@ams.com

CO-ORDINATORS
Dr. M. Santhosh,
Coordinator, Industry Institute Interactions,
msanthoshece@cvsr.ac.in
Phone: 9959856763
Mrs. S. Amrita,
IEEE CAS Student Branch Coordinator
amritaece@cvsr.ac.in
Phone:8499954678
Mr. P.Rama Krishna
Assoc. Prof. Dept. of ECE
Mr. E. Srinivas
Assoc. Prof. Dept. of ECE

REGISTRATION DETAILS
Non-IEEE Members – **Rs. 500/-**
IEEE Members – **Rs. 300/-**
Registration fee includes certificate of participation, lunch and snacks with registration kit.

REGISTRATION LINK
https://in.explara.com/e/workshop-on-analog-integrated-circuit-design-concept-to-reality
Prior registration is mandatory.

About the workshop:

Man-made Digital. God made Analog. Everything we see, feel, hear is an analog signal, which has a definite physical characteristics, frequency content and energy. In the process of extracting useful information in the presence of noisy unwanted signals, we need appropriate signal conditioning. Low-power and precision analog are necessary to design applications with higher performance and longer application lifetimes. The present workshop is designed to give a flavor of the entire IC product development flow and bridging the gap between real world requirements to IC requirements. This workshop is also intended to excite student and modern researchers to focus on VLSI and CMOS Analog IC Design.

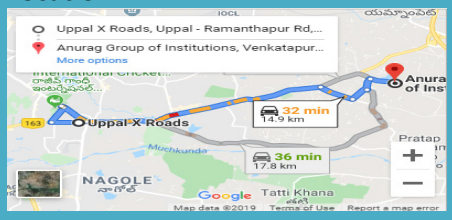
Resource Persons:

Dr. A.G.Krishna Kanth, Senior Manager, AMS Semiconductors, Vice-chair CAS/EDS chapter
Dr. V. Veeresh Babu, Manager, AMS Semiconductors, Member, CAS/EDS Chapter
S. Sudhakar, Manager, AMS Semiconductors
I. Harshitha, Team Lead, AMS Semiconductors

Date:
22nd - 23rd November 2019

Venue:
E-block Auditorium
Department of Electronics & Communications,
Anurag Group of Institutions,
Venkatapur, Ghatkesar Mandal,
Medchal District, Hyderabad,
Telangana, India 500 088.
website: https://anurag.edu.in/

Location:



https://goo.gl/maps/YE3kXfW9UyjU91a76

Detailed Schedule:

Schedule DAY 1 (22nd November 2019)	
Registration and Networking: 8.30 AM to 9.00 AM	
Analog IC Design Workshop Inaugural : 9.00 AM to 9.30 AM	
9:30AM – 12:30PM	Motivation, Economics of IC Design, Understanding system/application requirements, Research opportunities in Circuits and Systems
12:30PM – 1:30PM	LUNCH
1:30PM – 3:15PM	IC Architecture: Concept and Planning - Power partitioning, Analog/Digital Interface, Design Architecture, Test concept, Design for Specification, Pin-out, Package
3:20PM – 3:40PM	TEA BREAK
3:40PM – 5:15PM	Design for Test, Yield, Reliability/Quality, Robustness (ESD/EMI)
Schedule DAY 2 (23rd November 2019)	
9:00AM – 10:30AM	Practical Circuit design issues in Cadence Environment (Demo Session – CMOS Opamp design)
10:30AM – 10:45AM	TEA BREAK
10:45AM – 12:30PM	Demo session – CMOS Opamp design (contd.)
12:30PM – 1:30PM	LUNCH
1:30PM – 3:00PM	Layout and beyond... (GDS to Product), Demonstrations
3:00PM – 3:15PM	TEA BREAK
3:15PM – 4:45PM	Demonstrations contd., Validation ATE testing, Qualification and “Unlimited” production
4:45PM – 5:30PM	Closing ceremony