Course File Index

|  |  |  |
| --- | --- | --- |
| S.No. | Item Description | Page Number |
| 1 | Course Information Sheet |  |
| 2 | Syllabus |  |
| 3 | Text Books, Reference Book, Web/Internet Sources |  |
| 4 | Time Table |  |
| 5 | Programme Educational Objectives(PEO’s)&Programme Specific Outcomes (PSOs) |  |
| 6 | Programme Outcomes(PO’s) |  |
| 7 | Course Outcomes(CO’s), Mapping of Course Outcomes with PO’s, PEO’s |  |
| 8 | Articulation Matrix of COs and POs, Mapping of COs with PSO’s |  |
| 9 | Course Schedule |  |
| 10 | Lecture Plan / Teaching Plan |  |
| 11 | Unit Wise Date of Completion & Remarks |  |
| 12 | Unit Wise Assignment Questions |  |
| 13 | Unit Wise Very Multiple Choice Questions |  |
| 14 | Case Studies (2 In No.) with Level and Rubrics |  |
| 15 | Previous Question Papers |  |
| 16 | Tutorial Sheet |  |
| 17 | Topics Beyond Syllabus |  |
| 18 | Course Assessment Sheet (Direct & Indirect) |  |
| 19 | Add-on Programmes / Guest Lectures/Video Lectures& Remedial classes |  |
| 20 | Unit Wise PPT’s& Lecture Notes |  |

Course Coordinator HOD



Department of Computer Science and Engineering

 Course Name : Digital Logic Design

#  Course Number : A53024

#  Course Designation : Core

#  Prerequisites : Computer fundamentals

II B Tech – I Semester

# (2016-2017)

B. Ujwala

Assistant Professor

**SYLLABUS**

|  |  |
| --- | --- |
| **Unit – I** | **Number Systems:** Binary, Octal, Hex Decimal, and Conversions, range; Binary additions and subtractions (using 1c, and 2c), concept of overflow; representations of negative numbers using 1’s and 2’s complement and range; **BCD numbers:** Representation of 8421, 2421, Ex-3, Gray and self complementary codes; additions and subtractions on 8421 codes; **Error detecting codes:** even, odd parity, hamming codes; **Error correcting codes:** hamming codes, block parity codes; Floating point representation. |
| **Unit – II** | Boolean Algebra and Digital Logic GATES, Basic Boolean laws and properties; Boolean functions; canonical and standard forms (SOP, POS); Gate minimization using three and four variable K-Map’s with and without don’t cares. Encoders, Decoders, Multiplexers, D-Multiplexers;  |
| **Unit – III** | Definition of combinational circuits, design procedure for half, full, decimal (8421) adders and subtractors; Combinational Circuit Design for BCD code converters; |
| **Unit – IV** | Sequential circuits, latches, Flip Flops; Analysis of clocked sequential circuits, State Reduction and Assignment, Register, Ripple Counters, Synchronous Counters, Other Counters. |
| **Unit – V** | Types of Memory – Main memory – random access memory, ROM, Types of ROM; Decoder and RAM interface: Address lines, data lines, chip select signal; Design of large memories using small memories, using decoders; problems in memory design; Cache Memory- design issues, hit and miss ratio related problems; Associative and Auxiliary memory; |

**TEXT BOOKS & OTHER REFERENCES**

|  |
| --- |
| **Text Books** |
| 1. | Digital Design – Third Edition, M. Morris Mano, Pearson Education/PHI. |
| 2. | Fundamentals of Logic Design, Roth, Fifth Edition, Thomson. |
| **Suggested / Reference Books** |
| 3. | John F. Wakerly: Digital Design: Principles and Practices, 4th Edition, Pearson / Prentice Hall, 2005 |
| 4. | Digital Principles and Applications By Malvino& Leach, Seventh Edition, McGraw-Hill Education |
| 5 | Digital Electronics: Principles and Integrated Circuits By A.K. Maini, Wiley India Publications |
| 6 | Digital Design M. Morris Mano and Michael D. Ciletti, Pearson Education |

|  |
| --- |
| **Websites References**  |
|  | http://www.tutorialspoint.com/computer\_logical\_organization |
|  | https://www.tutorialspoint.com/videos/digital\_electronics |
|  | http://www.nesoacademy.org/ |

**Time Table**

Room No: W.E.F:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Class Hour****Time** | **1** | **2** | **3** | **4** | **12:20 – 1:10****LUNCH BREAK** | **5** | **6** | **7** |
| **9:00 -09:50** | **09.50 –10:40** | **10:40 –11:30** | **11:30 – 12: 20** | **1:10 –2:00** | **2:00 – 2:50** | **2:50 – 3:40** |
| **MON** |  |  |  |  |  |  |  |
| **TUE** |  |  |  |  |  |  |  |
| **WED** |  |  |  |  |  |  |  |
| **THU** |  |  |  |  |  |  |  |
| **FRI** |  |  |  |  |  |  |  |
| **SAT** |  |  |  |  |  |  |  |

**PROGRAM EDUCATIONAL OBJECTIVES (PEO’s)**

1. The graduates are employable as software professionals in reputed industries.
2. The graduates analyze problems by applying the principles of computer science, mathematics and scientific investigation to design and implement industry accepted solutions using latest technologies.
3. The graduates work productively in supportive and leadership roles on multidisciplinary teams with effective communication and team work skills with high regard to legal and ethical responsibilities.
4. The graduates embrace lifelong learning to meet ever changing developments in Computer Science and Engineering.

**PROGRAMME SPECIFIC OUTCOMES**

1. **Professional Skill:**The ability to understand, analyze and develop software

Solutions.

1. **Problem-Solving Skill:**The ability to apply standard principles, practices and

strategies for software development.

1. **Successful Career:** The ability to become Employee, Entrepreneur and /or Life

Long Leaner in the domain of Computer Science.

**PROGRAM OUTCOMES (PO’s)**

The Programme outcomes are the statements that describe the significant and essential learning that learners have achieved and can demonstrate at the end of the course or programme .The Programme Outcomes are the knowledge, skills and abilities that the student should acquire and posses during the graduation. The following are the list of Programme Outcomes to meet the Programme Educational Objectives

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization for the solution of complex engineering problems.
2. **Problem analysis:**  Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for public health and safety, and cultural, societal, and environmental considerations**.**
4. **Conduct investigations of complex problems:**  Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of t h e information to provide valid conclusions.
5. **Modern tool usage:**  Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modeling to complex engineering activities, with an understanding of the limitations.
6. **The engineer and society:**  Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal, and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability:**  Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with the society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance:**  Demonstrate knowledge and understanding of the engineering and management principles and apply these to one’s own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

**Course Outcomes:**

**After completion of the course the students will be able to:**

1. Make use of various number systems, error detecting and correcting codes.
2. Apply boolean algebraic principles and k-maps for simplification of boolean algebraic expressions.
3. Construct combinational circuits for various applications
4. Design sequential circuits for real time problems.
5. Compare various types of memories and their Usage.

**MAPPING OF COURSE OUT COMES WITH PO’s & PEO’s**

|  |  |  |
| --- | --- | --- |
| **Course Outcomes** | **PO’s** | **PEO’s** |
| 1 | 1,2,3,4,5,9 | 1,2,3,4 |
| 2 | 1,2,3,4,5 | 1,2,3,4 |
| 3 | 1,2,3,4,5 | 1,2,3,4 |
| 4 | 1,2,3,4,5,12 | 1,2,3,4 |
| 5 | 1,2 | 1,2,3 |

**Correlation of COs with Pos**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Cos** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | 2 | 3 | 3 | 2 | 2 | - | - | - | 1 | - | - | - |
| **CO2** | 2 | 2 | 3 | 2 | 1 | - | - | - | - | - | - | - |
| **CO3** | 2 | 3 | 3 | 2 | 1 | - | - | - | - | - | - | - |
| **CO4** | 3 | 2 | 3 | 2 | 3 | - | - | - | - | - | - | 2 |
| **CO5** | 1 | 1 | - | - | - | - | - | - | - | - | - | - |

**Correlation of COs with PSOs**

|  |  |  |  |
| --- | --- | --- | --- |
|  **PSOs** **Cos** | **PSO1** | **PSO2** | **PSO3** |
| 1 | 3 | 3 | 3 |
| 2 | 3 | 3 | 3 |
| 3 | 2 | 3 | 2 |
| 4 | 2 | 3 | 2 |
| 5 | 3 | 3 | 3 |

**COURSE SCHEDULE**

 **Distribution of Hours Unit – Wise**

|  |  |  |  |
| --- | --- | --- | --- |
| **Unit** | **Topic** | **Chapters** | **Total No. of Hours** |
| **Book1** | **Book2** |
| **I** | Number System, Error Detection and Error correction codes | Ch1 | Ch1 | 10 |
| **II** | Boolean algebra and K-Maps | Ch2,3 | Ch9 | 10 |
| **III** | Combinational Circuits | Ch4,5 | Ch8 | 8 |
| **IV** | Sequential Circuits | Ch6 | Ch11 | 9 |
| **V** | Memory | Ch7 | Ch9 | 8 |
| **Contact classes for Syllabus coverage** | **45** |
| Tutorial Classes : 05 ; Online Quiz : 1 Case studies-2 (Before Mid Examinations) Revision classes :1 per unit  |  |

|  |  |
| --- | --- |
| **Number of Hours / lectures available in this Semester / Year**  | **55** |

**Lecture Plan**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.No** | **Topic** | **Expected Date of Completion** | **Actual Date of Completion** | **Teaching Learning Process** |
| **Unit-I** |
| 1 | **Number Systems:** Binary, Octal, Hex Decimal Conversions, |  |  |  |
| 2 | Binary additions and subtractions (using 1c, and 2c) |  |  |  |
| 3 | Concept of overflow, representations of negative numbers using 1’s and 2’s complement and range; |  |  |  |
| 4 | Representation of 8421, 2421, Ex-3 |  |  |  |
| 5 | Gray and self complementary codes |  |  |  |
| 6 | Additions and subtractions on 8421 codes |  |  |  |
| 7 | **Error detecting codes:** even, odd parity, hamming codes; |  |  |  |
| 8 | Hamming codes |  |  |  |
| 9 | Block parity codes |  |  |  |
| 10 | Floating point representation |  |  |  |
| **Unit-II** |
| 1 | Boolean Algebra and Digital Logic GATES |  |  |  |
| 2 | Basic Boolean LAWs and properties |  |  |  |
| 3 | Boolean functions |  |  |  |
| 4 | Canonical forms  |  |  |  |
| 5 | Standard forms (SOP, POS) |  |  |  |
| 6 | Gate minimization using three and four variable K-Map’s with and without don’t cares |  |  |  |
| 7 |  Encoders, Decoders |  |  |  |
| 8 |  Multiplexers, D-Multiplexers;  |  |  |  |
| **Unit-III** |
| 1 | Definition of combinational circuits, Design procedure for half adders |  |  |  |
| 2 | Design procedure for full adders |  |  |  |
| 3 | Decimal (8421) adders  |  |  |  |
| 4 | Decimal (8421) sub tractors |  |  |  |
| 5 | Combinational Circuit Design for BCD code converters |  |  |  |
| **Unit-IV** |
| 1 | Sequential circuits |  |  |  |
| 2 |  Latches |  |  |  |
| 3 | Flip Flops |  |  |  |
| 4 | Analysis of clocked sequential circuits |  |  |  |
| 5 | State Reduction and Assignment |  |  |  |
| 6 | Registers |  |  |  |
| 7 | Ripple Counters |  |  |  |
| 8 | Synchronous Counters |  |  |  |
| 9 | Other Counters |  |  |  |
| **Unit-V** |
| 1 | Types of Memory – Main memory, Random access memory |  |  |  |
| 2 | ROM, Types of ROM |  |  |  |
| 3 | Decoder and RAM interface |  |  |  |
| 4 | Address lines, data lines, chip select signal |  |  |  |
| 5 | Design of large memories using small memories, problems in memory design |  |  |  |
| 6 | Cache Memory- design issues, hit and miss ratio related problems |  |  |  |
| 7 | Associative memory |  |  |  |
| 8 | Auxiliary Memory |  |  |  |
| **Total No of classes: 46** |

**Date of Unit Completion & Remarks**

|  |
| --- |
| **Unit – 1** |
| Date | : | \_\_\_ / \_\_\_ / \_\_\_ |
| Remarks:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |
| **Unit – 2** |
| Date | : | \_\_\_ / \_\_\_ / \_\_\_ |
| Remarks:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |
| **Unit – 3** |
| Date | : | \_\_\_ / \_\_\_ / \_\_\_ |
| Remarks:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |
| **Unit – 4** |
| Date | : | \_\_\_ / \_\_\_ / \_\_\_ |
| Remarks:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |
| **Unit – 5** |
| Date | : | \_\_\_ / \_\_\_ / \_\_\_ |
| Remarks:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |

**Unit Wise Assignments (With different Levels of thinking (Blooms Taxonomy))**

**Note: For every question please mention the level of Blooms taxonomy**

|  |
| --- |
| **Unit – 1** |
| 1. | Convert the following numbers [L3]a) (1432)8 to base 10 b) 10101100111.0101 to base 10c) 11010011001.1010 to base 8 and base 4d) (2002)10 to base 8 e) (2002)10 to base 6f) (75.125)10 to base 2 g) (3.375)10 to base 8 and base 2h) (ABCD)16 to base 10 |
| 2. | Perform the subtraction with the following unsigned binary numbers by taking the 2’s complement of the subtrahend. [L3] 1. 11010 - 10110
2. 11011 – 1001
3. 100 - 110100
4. 1010101 - 1010101
5. 11 - 1101.
 |
| 3. | Perform arithmetic operation indicated below. Follow signed bit notation: [L3] i. 001110 + 110010 ii. 101011 - 100110. |
| 4 | Illustrate Hamming code error detection and correction code.[L2] |
| 5 | Illustrate Floating point representation. [L2] |
| **Unit – 2** |
| 1. | 1. Find the complement of the Boolean function (BC’+A’D) (AB’+CD’) and reduce it to a minimum number of literals

(ii) Convert the function f (x, y, z) = π (0, 3, 6, 7) to the other canonical form. [L3] |
| 2. | Simplify the Boolean function F in sum of products using the don’t care conditions d: (Karnaugh map method) F = y’+x’z’ d = yz+xy. [L3] |
| 3. | Draw the AND-OR gate implementation of the following function after simplifying of the following function in SOP. F(A,B,C,D) = ∑ (0,2,5,6,7,8,10) [L3] |
| 4. | Simplify the following expression and implement them with two level NAND gate circuits. i)  ii) . [L3] |
| 5 | Simplify the Boolean function x′yz + x′yz′ + xy′z′ + xy′z using K-map. [L3] |
| **Unit – 3** |
| 1. | A combinational circuit has 4 inputs(A,B,C,D) and three outputs(X,Y,Z)XYZ represents a binary number whose value equals the number of 1's at the input. [L3] |
| 2. | (a)Implement Half adder using 4 NAND gates.(b) Implement full subtract or using NAND gates only. [L3] |
| 3. | (a) Design a BCD to Excess-3 code converter using minimum number of NAND gates(b) Design a BCD to Gray code converter using 8:1 multiplexers. [ L3] |
| 4 | Design a circuit with three inputs(A,B,C) and two outputs(X,Y) where the outputs are the binary count of the number of “ON" (HIGH) inputs [ L3] |
| 5 | Design a circuit with four inputs and one output where the output is 1 if the input is divisible by 3 or 7. [L3] |
| **Unit – 4** |
| 1. | Give the implementation of a 4-bit ripple-carry adder using half- adder(s) / full-adder(s). [L3] |
| 2. | Design A sequential circuit with two D flip flops A and B. and one input x. When x=0, the state of the circuit remains the same. When the x=1,the circuit goes through the state transition from 00 to 11 to 11 to 10 back to 00.and repeats.[L3] |
| 3. | Draw and explain with the help of truth table the logic diagram of a master slave D flip-flop using NAND gates. With active low preset and clear and with negative edge triggered clock.[L2] |
| 4. | Design a Modulo-12 up Synchronous counter sing T-Flip Flops and draw the circuit diagram.[L3] |
| 5. | Differentiate sequential and combinational circuits. [L2] |
| **Unit – 5** |
| 1. |  Design a circuit using ROM which will perform the squaring operation for the given 3 bit binary number.[L3] |
| 2. |  i. How many 32K \* 8 RAM chips are needed to provide a memory capacity of  256K bytes? [L3] ii. How many lines of the address must be used to access 256K bytes? How many of these lines are connected to the address inputs of all chips? iii. How many lines must be decoded for the chip select inputs? Specify the size of the decoder.  |
| 3 | Compare and contrast direct and associative mapping techniques in cache memory.[L2] |
| 4 | A computer uses RAM chips of 1024 x 1 capacity[L3] i)how many chips are needed and how should their address lines be connected to provide a  memory capacity of 16k bytes    ii)How many chips are needed to provide a memory capacity of 16 bytes |
| 5 | An eight way set associative cache consists of a total of 256 blocks. The main memory consists of 8192 blocks, each consisting of 128 words[L3]1. Calculate the number of bits in main memory address
2. Calculate the number of bits in TAG, SET and WORD fields
 |

**Case Studies (With Higher Levels of thinking (Blooms Taxonomy))**

**Note:For every Case Study please mention the level of Blooms taxonomy**

|  |
| --- |
| **1(Covering Syllabus Up to Mid-1)** |
| Design a circuit which with either Subtract X from Y or Y from X, depending on the value of A. If A=1, the output should be X-Y, & if A=0, the output should be Y-X. Use a 4-bit Subtractor and two 4 bit 2-to-1 multiplexer. [L3] |
| **2(Covering Entire Syllabus)** |
| Design a 3-bit up/down counter using J-K flip flops which counts up when the control signal M=1 and counts down when M=0 and draw the state diagram and state table.[L3] |

**Unit Wise Short Answer Questions**

|  |  |
| --- | --- |
| **Unit-1**1. | The number of digits in octal systems are----- |
| Ans. | 8 |  |

|  |  |
| --- | --- |
| 2. | The digit F in hexadecimal system has equivalence in digital system to-------- |
|  Ans. | 17 |  |
| 3. | The number FF in hexadecimal system has equivalence in decimal system to------ |
|  Ans. | 240 |  |

1. Two voltages are 0V and -5V. In positive logic ---------

 Ans. 0V is 1 and -5V is 0

|  |  |  |
| --- | --- | --- |
| 5. | In the decimal number 27, the digit 2 represents --- | ----- |
| Ans. | 20 |  |
| 6. | Hexadecimal number F is equal to octal number ------ |
| Ans. | 17 |  |  |  |

|  |  |  |
| --- | --- | --- |
| 7. | -8 is equal to signed binary number | (8 bit) ----------------- |
| Ans. | 10001000 |  |
| 8. | 1’ s complement of 11100110 is ----------- |  |
|  Ans. | 00011001 |  |
| 9. | 2’s complement of binary number 0101 is | ---------------- |
| Ans. | 1011 |  |
| 10. | -24 is 2’s complement form is ---------- |
| Ans. | 1000 |  |  |  |  |
| 11. | (E7F6)16 = (-----)10 |  |  |
| Ans. | (59382)10 |  |  |  |
| 12. | FF16 when converted to 8421 BCD is |  |
| Ans. | 0010 0101 0101 |  |
| 13. | Decimal number 9 in Gray code is ------- |  |
| Ans. | 1101 |  |

|  |  |  |
| --- | --- | --- |
| 14. | 11011 in gray code equal to binary |  |
| Ans. | (10010)2 |  |

**Unit – II**

1. Boolean algebra is also called ------------

2.  To perform product of maxterms Boolean function must be brought into -------

3. Boolean algebra theorem 6b gives x(x+y) equal to -----------

4. A Boolean function may be transformed into ---------

5.  e\*x=x\*e=x is the -----------------

6. Minterms are also called --------------------

7.  Maxterms are also called ----------------------

8. x+xy=x is known as --------------

9. A two valued Boolean algebra is defined as a set of -----------------

10. Most preceded operator is -------------- 11. (a+b+c)'= -------

12. A binary variable can take the values -------------

13. x+x' is equal to ----------

14. Demorgan law over addition is ----------------------

15. (x')' is --------------

**UNIT-III**

1. How many 3-line-to-8-line decoders are required for a 1-of-32 decoder?

|  |  |
| --- | --- |
| 2.  | Which of the figures shown below represents the exclusive-NOR gate?http://www.indiabix.com/_files/images/digital-electronics/digital-systems/mcq4_1012_1.gif |
|  |
| 3.  | Which of the circuits in figure (a to d) is the sum-of-products implementation of figure (e)?http://www.indiabix.com/_files/images/digital-electronics/digital-systems/mcq4_1021_1.gif |

|  |  |
| --- | --- |
| 4.  | For the device shown here, let all D inputs be LOW, both S inputs be HIGH, and the http://www.indiabix.com/_files/images/digital-electronics/digital-fundamentals/mcq6_01801.gifinput be LOW. What is the status of the Y output?http://www.indiabix.com/_files/images/digital-electronics/digital-fundamentals/mcq6_01802.gif |
|  |
| 5.  | For the device shown here, let all D inputs be LOW, both S inputs be HIGH, and the http://www.indiabix.com/_files/images/digital-electronics/digital-fundamentals/mcq6_01801.gifinput be HIGH. What is the status of the Y output?http://www.indiabix.com/_files/images/digital-electronics/digital-fundamentals/mcq6_01900.gif |
|  |
| 6. How many data select lines are required for selecting eight inputs? |
|  |

7. How many 1-of-16 decoders are required for decoding a 7-bit binary number?

8. For the device shown here, assume the D input is LOW, both S inputs are HIGH, and

 the  input is HIGH. What is the status of the  outputs?



|  |
| --- |
| 9. The device shown here is most likely a \_\_\_\_\_\_\_\_.http://www.indiabix.com/_files/images/digital-electronics/digital-fundamentals/mcq6_02000.gif |
|  |
| 10. How many 4-bit parallel adders would be required to add two binary numbers each representing decimal numbers up through 30010? |
|  |

**UNIT-IV**

**1**. A ripple counter's speed is limited by the propagation delay of:------------------

|  |  |
| --- | --- |
| **A.** | **each flip-flop** |

2. To operate correctly, starting a ring counter requires:--------------------------

|  |  |
| --- | --- |
| **A** | **presetting one flip-flop and clearing all the others** |

3. A comparison between ring and johnson counters indicates that:-------------------

|  |  |
| --- | --- |
| **A** | **a johnson counter has an inverted feedback path** |

4. A sequence of equally spaced timing pulses may be easily generated by which type of counter circuit?

|  |  |
| --- | --- |
| **A.** | **shift register sequencer** |

5. What is meant by parallel-loading the register?

|  |  |
| --- | --- |
| **A** | **Loading data in all four flip-flops at the same time** |

6. What is a shift register that will accept a parallel input and can shift data left or right called?

|  |  |
| --- | --- |
| **A.** | **bidirectional universal** |

7. SR latch consists of-----

1. **2 inputs**

8. Outputs of SR latch are-----------

1. **q and q'**

**9.** NAND latch works when both inputs are

1. **1**

 10. Inputs of SR latch are-----

1. **s and r**

**UNIT-V**

|  |
| --- |
| 1. How many address bits are needed to select all memory locations in the 2118 16K × 1 RAM? |
|

|  |  |  |  |
| --- | --- | --- | --- |
| A. | **14** |  |  |

 |

**2.**What is the meaning of RAM, and what is its primary role?

|  |  |
| --- | --- |
| A. | **Random Access Memory; it is the memory used for short-term temporary data storage within the computer.** |

3. The storage element for a static RAM is the \_\_\_\_\_\_\_\_.

|  |  |  |  |
| --- | --- | --- | --- |
| A. | **flip-flop** |  |  |

4.A 64-bit word consists of \_\_\_\_\_\_\_\_.

|  |  |
| --- | --- |
| **A.** | **8 bytes** |

5.Select the statement that best describes Read-Only Memory (ROM).

|  |  |
| --- | --- |
| **A.** | **nonvolatile, used to store information that does not change during system operation** |

6.How many 2K × 8 ROM chips would be required to build a 16K × 8 memory system?

|  |  |  |  |
| --- | --- | --- | --- |
| **C.** | **8** |  |  |

7.How many storage locations are available when a memory device has 12 address lines?

|  |  |  |  |
| --- | --- | --- | --- |
|  | A. **4096** |  |  |

8.**The idea of cache memory is based \_\_\_\_\_\_.**

**A.      on the property of locality of reference**

9. The algorithm to remove and place new contents into the cache is called \_\_\_\_\_\_\_.
a) **Replacement algorithm**

10. The method of mapping the consecutive memory blocks to consecutive cache blocks is called \_\_\_\_\_\_.
A. **Direct**

11. While using the direct mapping technique, in a 16 bit system the higher order 5 bits is used for \_\_\_\_\_\_\_\_.
A. **Tag**

12. In direct mapping the presence of the block in memory is checked with the help of block field.
A. **False**

13. In associative mapping, in a 16 bit system the tag field has \_\_\_\_\_\_ bits.
A. **12**

14. The associative mapping is costlier than direct mapping ( State True/False).
A. **True**

15. The technique of searching for a block by going through all the tags is \_\_\_\_\_\_.
A. **Associative search**

**Tutorial Sheet**

|  |  |
| --- | --- |
| **Date:** | **Topics Revised** |
| **Date:** | **Topics Revised** |
| **Date:** | **Topics Revised** |
| **Date:** | **Topics Revised** |
| **Date:** | **Topics Revised** |

**TOPICS BEYOND SYLLABUS**

|  |  |
| --- | --- |
| S.No.  | Topic |
| 1 |  |
| 2 |  |
| 3. |  |

**ASSESMENT OF COURSE OUTCOMES: DIRECT**

**Blooms Taxonomy:**

|  |  |  |
| --- | --- | --- |
| **LEVEL 1**  | **REMEMBERING** | Exhibit memory of previously learned material by recalling facts, terms, basic concepts, and answers |
| **LEVEL 2**  | **UNDERSTANDING** | Demonstrate understanding of facts and ideas by organizing, comparing, translating, interpreting, giving descriptions, and stating main ideas. |
| **LEVEL 3**  | **APPLYING** | Solve problems to new situations by applying acquired knowledge, facts, techniques and rules in a different way |
| **LEVEL 4**  | **ANALYZING** | Examine and break information into parts by identifying motives or causes. Make inferences and find evidence to support generalizations. |
| **LEVEL 5**  | **EVALUATING** | Present and defend opinions by making judgments about information, validity of ideas, or quality of work based on a set of criteria. |
| **LEVEL 6**  | **CREATING** | Compile information together in a different way by combining elements in a new pattern or proposing alternative solutions. |

**\*Attach course assessment sheet**

 **ASSESMENT OF COURSE OUTCOMES: INDIRECT**

|  |
| --- |
| **CSP Rubric** |
| S.N0 | Criteria | **LEVEL**  ( Level : 3-Excellent Level :2-Good Level : 1-Poor) |
| 1 | **Oral Communication** | 3 | Student speaks in phase with the given topic confidently using Audio-Visual aids. Vocabulary is good |
| 2 | Student speaking without proper planning, fair usage of Audio-Visual aids. Vocabulary is not good |
| 1 | Student speaks vaguely not in phase with the given topic. No synchronization among the talk and Visual Aids |
| 2 | **Writing Skills** | 3 | Proper structuring of the document with relevant subtitles, readability of document is high with correct use of grammar. Work is genuine and not published anywhere else |
| 2 | Information is gathered without continuity of topic, sentences were not framed properly. Few topics are copied from other documents |
| 1 | Information gathered was not relevant to the given task, vague collection of sentences. Content is copied from other documents |
| 3 | **Social and Ethical Awareness**  | 3 | Student identifies most potential ethical or societal issues and tries to provide solutions for them discussing with peers |
| 2 | Student identifies the societal and ethical issues but fails to provide any solutions discussing with peers |
| 1 | Student makes no attempt in identifying the societal and ethical issues |
| 4 | **Content Knowledge** | 3 | Student uses appropriate methods, techniques to model and solve the problem accurately |
| 2 | Student tries to model the problem but fails to solve the problem |
| 1 | Student fails to model the problem and also fails to solve the problem |
| 5 | **Student Participation** | 3 | Listens carefully to the class and tries to answer questions confidently |
| 2 | Listens carefully to the lecture but doesn’t attempt to answer the questions |
| 1 | Student neither listens to the class nor attempts to answer the questions |
| 6 | **Technical and analytical Skills** | 3 | The program structure is well organized with appropriate use of technologies and methodology. Code is easy to read and well documented. Student is able to implement the algorithm producing accurate results |
| 2 | Program structure is well organized with appropriate use of technologies and methodology. Code is quite difficult to read and not properly documented. Student is able to implement the algorithm providing accurate results. |
| 1 | Program structure is not well organized with mistakes in usage of appropriate technologies and methodology. Code is difficult to read and student is not able to execute the program |
| 7 | **Practical Knowledge** | 3 | Independently able to write programs to strengthen the concepts covered in theory |
| 2 | Independently able to write programs but not able to strengthen the concepts learned in theory |
| 1 | Not able to write programs and not able to strengthen the concepts learned in theory |
| 8 | **Understanding of Engineering core** | 3 | Student uses appropriate methods, techniques to model and solve the problem accurately in the context of multidisciplinary projects  |
| 2 | Student tries to model the problem but fails to solve the problem in the context of multidisciplinary projects |
| 1 | Student fails to model the problem and also fails to solve the problem in the context of multidisciplinary projects |

**Guest Lectures:**

* 1. Organized Guest Lecture on 06/10/2016 on practical demonstration of Gates, Multiplexers, and Counters

**Unit Wise PPT’s:**

PPTs Available

**Unit Wise lecture Notes:**

 **LECTURE NOTES AVAILABLE**