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**COURSE COORDINATOR HOD**



#  Course Name : Computer Organization

#  Course Number : A54025

#  Course Designation :Core

#  Prerequisites : Digital Logic Design

# II B Tech – II Semester

# (2016-2017)

05th Dec 2016 to 05thApril 2017

Mrs.P. VinayaSree

Assistant Professor

Course Coordinator

**SYLLABUS**

|  |  |
| --- | --- |
| **Unit – I** | Instruction definition ,instruction cycle, instruction storage, types of instruction formats(Zero, one, two, three address)addressing modes, mode filed ,implied, immediate register, register direct, register indirect, auto increment, decrement, indexed, relative, base address mode, numerical example and problems. |
| **Unit – II** | **CPU-Organization:** 8086 – CPU – Block diagram and pin diagram, concept of pipelining, minimum and maximum mode, General purpose registers; segment register and generation of 20 bits address, segmentation of main memory, Addressing modes, systems bus, Types of flags. |
| **Unit – III** | Memory Hierarchy, Main memory, memory address map, memory connection to CPU; auxiliary memory, Magnetic disks, magnetic tapes; cache memory, hit and miss ratio, direct, associative and set associative mapping; Micro-programmed control: control memory, address sequencing. |
| **Unit – IV** | **I/O interface:** I/O Bus and Interface modules, I/O versus Memory Bus, isolated vs Memory mapped I/O. Asynchronous data transfer-strobe control, Hand shaking; Modes of Transfer:Example of programmed I/O, interrupt-initiated I/O, software considerations. Daisy-Chaining priority. DMA: DMA Controller, DMA Transfer, Intel 8089 IOP. |
| **Unit – V** | MULTIPROCESSORS: characteristic of multi processor, interconnection structure,: time shared common bus, multiport memory, cross bar Switch, multistage switching network, introduction to Flynn’s classification: SISD,SIMD,MISDMIMD(Introduction). |

**TEXT BOOKS& OTHER REFERENCES BOOKS**

|  |
| --- |
| **Text Books** |
| 1. | Computer Systems and Architecture –M.MorrisMano,Third Edition, Pearson /PHI,2011 |
| 2. | Microprocessor and interfacing –Douglass V. Hall 2nd edition McGraw-Hill |
| **Suggested / Reference Books** |
| 1. | **C.** Hamacher, Z. Vranesic and S. Zaky, "Computer Organization", McGraw-Hill, 2002.  |
| 2. | W. Stallings, "Computer Organization and Architecture - Designing for Performance", Prentice Hall of India, 2002 |
| 3. | J .P. Hayes, "Computer Architecture and Organization", McGraw-Hill, 1998 |

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| **Websites References**  |
|  | <https://en.wikibooks.org/wiki/IB/Group_4/Computer_Science/Computer_Organisation> |
|  | <http://www.cs.uwm.edu/classes/cs458/Lecture/HTML/ch05.html> |
|  | <http://www.cse.iitm.ac.in/~vplab/courses/comp_org.htm> |

**Time Table**

Room **No:** A –Block-113 **W.E.F:**15-12-2016 to 5-04-2017

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Class HourTime | **1** | **2** | **3** | **4** | **12:20 – 1:10****LUNCH BREAK** | **5** | **6** | **7** |
| **9:00 -09:50** | **09.50 –10:40** | **10:40 –11:30** | **11:30 – 12: 20** | **1:10 – 2:00** | **2:00 – 2:50** | **2:50 – 3:40** |
| MON |  |  |  |  | COII CSE-D |  |  |
| TUE |  |  | COII CSE-D |  |  |  |  |
| WED | COII CSE-D |  |  |  |  |  |  |
| THU |  |  |  |  |  |  |  |
| FRI |  |  |  |  |  |  |  |
| SAT |  |  | COII CSE-D |  |  |  |  |

**Program Educational Objectives (PEO’s)**

|  |  |
| --- | --- |
| **PEO1:** | The Graduates are employable as software professionals in reputed industries. |
| **PEO2:** | The Graduates analyze problems by applying the principles of computer science, mathematics and scientific investigation to design andimplement  industry accepted solutions using latest technologies. |
| **PEO3:** | The Graduates work productively in supportive and leadership roles on multidisciplinary teams with effective communication and team work skills with high regard to legal and ethical responsibilities. |
| **PEO4:** | The Graduates embrace lifelong learning to meet ever changing developments in computer science and Engineering. |

**Program Specific Outcomes(PSO’s)**

**PSO1: Professional Skill:** The ability to understand, analyze and develop software solutions

**PSO2: Problem-Solving Skills:** The ability to apply standard principles, practices and strategies for software development

**PSO3: Successful Career:** The ability to become Employee, Entrepreneur and/or Life Long Leaner in the domain of Computer Science.

**Program Outcomes (PO’s)**

1. **Engineering    knowledge:**    Apply   the   knowledge   of mathematics, science, engineering fundamentals, and an engineering specialization for the solution of complex engineering problems.
2. **Problem  analysis:**  Identify,  formulate,  research  literature,  and   analyze   complex  engineering problems reaching substantiated conclusions  using  first  principles  of mathematics, natural sciences,  and  engineering sciences.
3. **Design/development of solutions:** Design solutions for complex engineering problems and  design system components or   processes  that  meet  the  specified needs  with  appropriate consideration  for   public  health   and  safety, and cultural,  societal, and environmental considerations.
4. **Conduct investigations of   complex   problems:**   Use research-based knowledge and    research methods including design of   experiments,   analysis   and   interpretation of   data,   and   synthesis   of   the    information   to   provide   valid   conclusions.
5. **Modern tool usage:** Create, select,   and   apply   appropriate techniques,   resources, and   modern   engineering and   IT   tools, including   prediction and modeling to   complex   engineering activities,   with   an   understanding of the limitations.
6. **The   engineer and society:** Apply reasoning informed    by the contextual knowledge to  assess  societal,  health,  safety, legal, and  cultural  issues  and  the  consequent responsibilities relevant to the professional engineering practice.
7. **Environment   and   sustainability:**   Understand   the   impact   of   the professional   engineering    solutions     in    societal    and environmental contexts,    and demonstrate the   knowledge of, and need for sustainable development.
8. **Ethics:**   Apply   ethical   principles   and   commit   to   professional   ethics   and   responsibilities and norms of the engineering practice.
9. **Individual  and  team  work:**  Function   effectively  as  an  individual,  and   as  a  member or leader  in diverse teams, and  in multidisciplinary  settings.
10. **Communication:**  Communicate  effectively  on complex  engineering activities with  the engineering community and  with  the   society  at  large,  such  as,  being    able to    comprehend and    write    effective reports and design documentation, make   effective   presentations, and   give   and   receive   clear   instructions.
11. **Project management and  finance:** Demonstrate knowledge and understanding of  the   engineering  and  management  principles  and   apply  these  to  one’s  own  work,  as  a  member  and  leader  in  a  team,  to  manage projects  and  in  multidisciplinary  environments.
12. **Life-long  learning:**  Recognize  the  need  for,  and  have  the  preparation and ability to  engage in independent and  life-long  learning   in  the   broadest  context  of technological change.

**Course Outcomes:**

Upon successful completion of this course, students will be able to:

**CO1:** Understand the basic organization of computer and different instruction formats and addressing modes.

**CO2:** Analyze the concept of pipelining, segment registers and pin diagram of CPU.

**CO3:** Understand and analyze various issues related to memory hierarchy.

**CO4:** Evaluate various modes of data transfer between CPU and I/O devices.

**CO5:** Examine various inter connection structures of multi processors.

**Mapping of Course out Comes With PO’s & PEO’s**

|  |  |  |
| --- | --- | --- |
| **Course Outcomes** | **PO’s** | **PEO’s** |
| CO1 | 1,2,7,5,12 | 2 |
| CO2 | 1,2,4,5,12 | 2 |
| CO3 | 1,2,4,5,7,12 | 3,4 |
| CO4 | 1,2,3,4,7,12 | 4 |
| CO5 | 1,2,3,5,9,12 | 4 |

**Course Attriculation Matrix:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **CO’s/PO’s** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **P10** | **PO11** | **PO12** |
| **CO1** | 3 | 3 |  |  | 3 |  | 2 |  |  |  |  | 2 |
| **CO2** | 3 | 3 |  | 3 | 2 |  |  |  |  |  |  | 3 |
| **CO3** | 3 | 3 |  | 3 | 2 |  | 2 |  |  |  |  | 2 |
| **CO4** | 3 | 2 | 3 | 2 |  |  | 2 |  |  |  |  | 3 |
| **CO5** | 3 | 3 | 3 |  | 2 |  |  |  | 3 |  |  | 2 |

**Mapping of Course outcomes to PSO’s:**

|  |  |  |  |
| --- | --- | --- | --- |
| **COURSE** | **PSO1** | **PSO2** | **PSO3** |
| CO1 | 2 | 3 | 2 |
| CO2 | 3 | 3 | 2 |
| CO3 | 3 | 3 | 2 |
| CO4 | 3 | 2 | 1 |
| CO5 | 3 | 3 | 1 |

**Course Schedule**

**Distribution of Hours Unit – Wise**

|  |  |  |  |
| --- | --- | --- | --- |
| **Unit** | **Topic** | **Chapters** | **Total No. of Hours** |
| **Book1** | **Book2** |
| **I** | Instruction Cycle ,Addressing Modes | Ch5,8 |  | 10 |
| **II** | CPU organization | Ch9 |  | 8 |
| **III** | Memory Hierarchy, Cache memory mapping techniques micro programmed control | Ch6,7 | Ch6 | 10 |
| **IV** | I/O bus and interface modules | Ch11 |  | 10 |
| **V** | Multiprocessors | Ch13 |  | 10 |
| **Contact classes for Syllabus coverage** | **48** |
| Tutorial Classes : 05 ; Online Quiz : 1 Case studies-2 Revision classes :1 per unit  |  |

**Number of Hours / lectures available in this Semester / Year 64**

**The number of topic in every unit is not the same – because of the variation, all the units have an unequal distribution of hours**

**Teaching Plan**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S. No.** | **Topic** | **Expected Date of Completion** | **Actual Date of Completion** | **Teaching Learning Process** |
| **Unit-I** |
| 1 | Instruction definition ,instruction cycle | 6-12-2016 |  | Animated video |
| 2 | Instruction Storage, Types Of Instruction Formats | 08-12-2016 |  | PPT |
| 3 | Zero address and One address Instruction Formats | 09-12-2016 |  |  |
| 4 | Two and Three address Instruction Formats | 10-12-2016 |  |  |
| 5 | Addressing Modes, Mode Filed | 13-12-2016 |  | PPT |
| 6 | Implied, immediate register, register direct, register Indirect | 15-12-2016 |  | PPT |
| 7 | Auto Increment, Decrement, Indexed, Relative, Base Address Mode | 16-12-2016 |  | PPT |
| 8 | Indexed, Relative, Base Address Mode  | 19-12-2016 |  | PPT |
| 9 | Numerical example and problems. | 20-12-2016 |  |  |
| 10 | REVIEW | 21-12-2016 |  |  |
| **Unit-II** |
| 1 | CPU organization:8086-CPU-block diagram  | 22-12-2016 |  | PPT |
| 2 | Pin diagram | 20-12-2016 |  | PPT |
| 3 | concept of pipelining, | 23-12-2016 |  | PPT |
| 4 | Minimum And Maximum Mode | 24-12-2016 |  |  |
| 5 | Generation of 20 bit address, data | 26-12-2016 |  |  |
| 6 | data, control and synchronous bus | 27-12-2016 |  |  |
| 7 | Segment Register, And Types Of Flags | 28-12-2016 |  |  |
| 8 | REVIEW | 29-12-2016 |  |  |
| **Unit-III** |
| 1 | Memory Hierarchy, Main memory | 30-12-2016 |  | PPT |
| 2 | Memory Address Map | 31-12-2016 |  |  |
| 3 | Memory connection to CPU | 02-01-2017 |  |  |
| 4 | Auxiliary memory, Magnetic disks, Magnetic tapes | 03-01-201704-01-2017 |  |  |
| 5 | Cache memory, hit and miss ratio | 05-01-2017 |  | Video Lecture |
| 6 | Direct mapping | 08-01-2017 |  | Video Lecture |
| 7 | Associative and Set Associative mapping | 09-01-2017 |  | Video Lecture |
| 8 | Micro-programmed control: control memory | 11-01-2017 |  |  |
| 9 | Micro-programmed control: address sequencing | 13-01-2017 |  |  |
| 10 | REVIEW | 16-01-2017 |  |  |
| **Unit-IV** |
| 1 | I/O Interface | 19-01-2017 |  |  |
| 2 | I/O bus and interface modules | 21-01-2017 |  |  |
| 3 | I/O versus memory bus | 23-01-2017 |  |  |
| 4 | Isolated vs Memory mapped I/O. | 24-01-2017 |  |  |
| 5 | Asynchronous data transfer-strobe control, Hand shaking | 30-01-2017 |  | PPT |
| 6 | Modes of Transfer: Example of Programmed I/O | 06-02-2017 |  |  |
| 7 | Interrupt-Initiated I/O, Software considerations | 07-02-2017 |  |  |
| 8 | Daisy-Chaining priority. DMA : DMA controller | 08-02-2017 |  |  |
| 9 | DMA transfer, Intel 8089,IOP | 13-02-2017 |  |  |
| 10 | REVIEW | 14-02-2017 |  |  |
| **Unit-V** |
| 1 | MULTIPROCESSORS: characteristic of multi-processor | 27-02-2017 |  | PPT |
| 2 | Interconnection Structure | 28-02-2017 |  |  |
| 3 | Time shared common bus | 06-03-2017 |  |  |
| 4 | Multiport Memory | 14-03-2017 |  |  |
| 5 | Cross bar Switch | 22-03-2017 |  |  |
| 6 | Multistage switching network | 25-03-2017 |  |  |
| 7 | Introduction To Flynn’s Classification | 27-03-2017 |  | PPT |
| 8 | SISD,SIMD | 28-03-2017 |  |  |
| 9 | MISD,MIMD(Introduction) | 30-03-2017 |  |  |
| 10 | REVIEW | 31-03-2017 |  |  |
|  | **Total No Of Hrs Required For The Course:48** |  |

**Date of Unit Completion & Remarks**

|  |
| --- |
| **Unit – 1** |
| Date | : | \_\_ / \_\_ / \_\_ |
| Remarks:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |
| **Unit – 2** |
| Date | : | \_\_ / \_\_ / \_\_ |
| Remarks:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |
| **Unit – 3** |
| Date | : | \_\_ / \_\_ / \_\_ |
| Remarks:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |
| **Unit – 4** |
| Date | : | \_\_ / \_\_ / \_\_ |
| Remarks:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |
| **Unit – 5** |
| Date | : | \_\_ / \_\_ / \_\_ |
| Remarks:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |

**Unit Wise Assignments (With different Levels of thinking – Blooms Taxonomy and Course Outcomes)**

|  |
| --- |
| **Unit – 1** |
| 1. | With a neat flow chart explain instruction execution.[L2,CO-1] |
| 2. | How the operation X = (A + B) \* (C + D) / (E+F) is performed using:a) Three address instruction b) Two address instructionc) One address instruction d) zero address instruction [L3,CO-1] |
| 3. | Analyze different addressing modes.[L4,CO-1] |
| 4 | 1. How many bits are there in the operation code, register code part, and address part?
2. Draw the instruction word format and indicate the number of bits in each part.
3. How many bits are there in the data and address inputs of memory?[L1,CO-1]
 |
| **Unit – 2** |
| 1. | Draw the pin diagram of 8086 and explain each one.[L2,CO-2] |
| 2. | Explain how different types of registers in 8086 microprocessor architecture are functioning compare among them?[L2,CO-2] |
| 3. | What is the minimum number of segment resisters that are necessary to provide segmentation? How do you access common data for different programs using segmentation? [L1,CO-2] |
| 4. | List the signals in minimum and List the signals in minimum modes.[L1,CO-2] |
| 5. | What happens to the SI, DI, and CX registers when the MOVSB instruction is executed (without a repeat prefix) and:1. the direction flag is set
2. ii. the direction flag is clear.[L1,CO-2]
 |
| **Unit – 3** |
| 1. | What are the different types of magnetic memory? Describe them briefly [L2,CO-3]? |
| 2. |  Explain Cache memory Mapping Techniques.[L2,CO-3] |
| 3. | How the micro program sequencer determines address of the next micro instruction to be executed.[L4,CO-3] |
| 4. | Compare and contrast Hard wired control unit and Micro programmed control.[L4,CO-3] |
| **Unit – 4** |
| 1. | Analyze different modes of transfer[L2,CO-4] |
| 2. | a) What is meant by asynchronous data transfer? Explain Strobe control and Handshaking methods.[L1,CO-4]b) Why does DMA have priority over the CPU when both request a memory transfer?[L1,CO-4] |
| 3. | Explain working of Direct Memory Access Controller.[L2,CO-4] |
| 4. | Write the difference between Isolated I/O and Memory Mapped I/O.[L5,CO-4] |
| **Unit – 5** |
| 1. | Explain about Multiprocessor Architecture and Applications.[L2,CO-5] |
| 2. | Explain Flynn’s classification of computers.[L2,CO-5] |
| 3. | Define the following: (i) Crossbar switch (ii) Multistage switch.[L1,CO-5] |
| 4. | Construct an 8\*8 Omega switching network using 2\*2 interchange switch.[L5,CO5] |

**Unit Wise Short Answer Questions (With different Levels of thinking – Blooms Taxonomy)**

**Unit – I:**

1. Explain the importance of different addressing modes in computer architecture with suitable example[L2]
2. What is an instruction format? Explain different types of instruction formats in detail.[L1]
3. What is an instruction code? Explain in detail various addressing modes[L1]
4. Explain the instruction cycle with a neat flow chart.[L2]

**Unit – II:**

1. With examples ,explain how multiplexing is implemented in 8086 Microprocessor[L2]
2. Explain the roles of pins TEST, LOCK. [L2]
3. Which are the pins of 8086 that are to be connected to interface 8284 and explain their functions? [L2]
4. Explain briefly about memory interfacing with 8086 microprocessor. [L2]

**Unit – III:**

1. Explain memory hierarchy in a computer system. [L2]
2. Explain memory hierarchy in a computer system. [L2]
3. What is the difference between microprocessor and a micro program?[L1]
4. Explain Cache memory mapping techniques[L2]

**Unit – IV:**

1. What is the basic advantage of using interrupt initiated data transfer over transfer under program control without an interrupt?[L1]
2. What is direct memory access (DMA)? Why are the read and write control lines in a DMA controller bi directional? [L1]
3. What is the basic advantage of using interrupt initiated data transfer over transfer under program control without an interrupt? What is asynchronous data transfer? Explain in detail[L1]
4. What is asynchronous data transfer? Explain in detail[L1]
5. What is the difference between isolated I/O and memory mapped I/O? [L1]

**Unit – V:**

1. Explain Flynn’s classification of computers. [L2]
2. Explain about Multiprocessor Architecture and Applications. [L2]
3. Define the following: (i) Crossbar switch (ii) Multistage switch. [L1]
4. List the types of interconnection structure. [L2]
5. Construct 2\*2 crossbar switch network.[L3]
6. Explain 2\*2 interchange switch.[L2]
7. List the characteristics of Multiprocessors.[L2]

**Case Studies (With Higher Levels of thinking (Blooms Taxonomy))**

|  |
| --- |
| **1(Covering Syllabus Up to Mid-1)** |
| The content of PC in the basic computer is 3AF. The content of AC is 7EC. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 09ac is 8B9F.1. What is the instruction that will be fetched and executed next?[L1]
2. Show the binary operation that will be performed in the AC when the instruction is executed.[L2]
3. Give the contents of registers PC,AR, DR, AC, and IR in hexadecimal and the value of E, I, and sequence counter SC in binary at the end of the instruction cycle

 [Content Knowledge]. Rubric 4 |
| **2(Covering Entire Syllabus)** |
| 2. Consider a bus topology in which two processors communicate through a buffer in shared memory. When one processor wishes to communicate with the other processor it puts the information in the memory buffer and set a flag. Periodically, the other processor checks the flags to determine if it has information to receive. What can be done to ensure proper synchronization and to minimize the time between sending and receiving the information? [Content Knowledge]. Rubric 4 |

**Previous Question Papers**

**Tutorial Sheet**

|  |
| --- |
| **Unit-I Topics Revised** |
| **Topic Name** | **Date** |
|  |  |
|  |  |
|  |  |
| **Unit-II Topics Revised**  |
| **Topic Name** | **Date** |
|  |  |
|  |  |
|  |  |
| **Unit-III Topics Revised**  |
| **Topic Name** | **Date** |
|  |  |
|  |  |
|  |  |
| **Unit-IV Topics Revised**  |
| **Topic Name** | **Date** |
|  |  |
|  |  |
|  |  |
| **Unit-V Topics Revised**  |
| **Topic Name** | **Date** |
|  |  |
|  |  |
|  |  |

**Topics Beyond Syllabus**

|  |  |
| --- | --- |
| **S.No.**  | **Topic** |
| 1 | Common Bus System, CPU Organizations, Interrupt Cycle[L2] |
| 2 | Instruction Set(CISC,RISC)[L2] |
| 3. | Data Hazards ,Instruction Hazards[L2] |
| 4. | Hardwired Control Unit[L2] |

**Course Assessment Sheet**

**Batch:**

**Academic Year/Sem:**

**Course Name:**

**Course Number:**

**Course Attainment = 75% of Direct + 25% of Indirect=**

**Remarks and suggestions:**

 1 - Slight 2 - Moderate 3 – Substantial

**Course Coordinator**

**Blooms Taxonomy Direct**

|  |  |  |
| --- | --- | --- |
| **Level 1**  | **Remembering** | Exhibit memory of previously learned material by recalling facts, terms, basic concepts, and answers. |
| **Level 2**  | **Understanding** | Demonstrate understanding of facts and ideas by organizing, comparing, translating, interpreting, giving descriptions, and stating main ideas. |
| **Level 3** | **Applying** | Solve problems to new situations by applying acquired knowledge, facts, techniques and rules in a different way. |
| **Level 4**  | **Analyzing** | Examine and break information into parts by identifying motives or causes. Make inferences and find evidence to support generalizations. |
| **Level 5**  | **Evaluating** | Present and defend opinions by making judgments about information, validity of ideas, or quality of work based on a set of criteria. |
| **Level 6**  | **Creating** | Compile information together in a different way by combining elements in a new pattern or proposing alternative solutions. |

**Direct Course Assessment Sheet**

1. **Internal Examination**

**Course assessment sheet Mid1**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Hall Ticket No** | **S1** | **S2** | **S3** | **S4** | **S5** | **L1** | **L2** | **L3** | **L4** | **L5** | **ASS** | **TOT** |
| 1 |  |  |  |  |  |  |  |  |  |  |  |  |
| 2 |  |  |  |  |  |  |  |  |  |  |  |  |
| 3 |  |  |  |  |  |  |  |  |  |  |  |  |

**Course assessment sheet Mid2**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Hall Ticket No** | **S1** | **S2** | **S3** | **S4** | **S5** | **L1** | **L2** | **L3** | **L4** | **L5** | **ASS** | **TOT** |
| 1 |  |  |  |  |  |  |  |  |  |  |  |  |
| 2 |  |  |  |  |  |  |  |  |  |  |  |  |
| 3 |  |  |  |  |  |  |  |  |  |  |  |  |

1. **External Examination**

|  |  |
| --- | --- |
| **Hall Ticket No** | **Total Marks** |
|  |  |
|  |  |
|  |  |

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| --- |
| **CSP Rubric** |
| S.No. | Criteria | **LEVEL**  ( Level : 3-Excellent Level :2-Good Level : 1-Poor) |
| 1 | **Oral Communication** | 3 | Student speaks in phase with the given topic confidently using Audio-Visual aids. Vocabulary is good |
| 2 | Student speaking without proper planning, fair usage of Audio-Visual aids. Vocabulary is not good |
| 1 | Student speaks vaguely not in phase with the given topic. No synchronization among the talk and Visual Aids |
| 2 | **Writing Skills** | 3 | Proper structuring of the document with relevant subtitles, readability of document is high with correct use of grammar. Work is genuine and not published anywhere else |
| 2 | Information is gathered without continuity of topic, sentences were not framed properly. Few topics are copied from other documents |
| 1 | Information gathered was not relevant to the given task, vague collection of sentences. Content is copied from other documents |
| 3 | **Social and Ethical Awareness**  | 3 | Student identifies most potential ethical or societal issues and tries to provide solutions for them discussing with peers |
| 2 | Student identifies the societal and ethical issues but fails to provide any solutions discussing with peers |
| 1 | Student makes no attempt in identifying the societal and ethical issues |
| 4 | **Content Knowledge** | 3 | Student uses appropriate methods, techniques to model and solve the problem accurately |
| 2 | Student tries to model the problem but fails to solve the problem |
| 1 | Student fails to model the problem and also fails to solve the problem |
| 5 | **Student Participation** | 3 | Listens carefully to the class and tries to answer questions confidently |
| 2 | Listens carefully to the lecture but doesn’t attempt to answer the questions |
| 1 | Student neither listens to the class nor attempts to answer the questions |
| 6 | **Technical and analytical Skills** | 3 | The program structure is well organized with appropriate use of technologies and methodology. Code is easy to read and well documented. Student is able to implement the algorithm producing accurate results |
| 2 | Program structure is well organized with appropriate use of technologies and methodology. Code is quite difficult to read and not properly documented. Student is able to implement the algorithm providing accurate results. |
| 1 | Program structure is not well organized with mistakes in usage of appropriate technologies and methodology. Code is difficult to read and student is not able to execute the program |
| 7 | **Practical Knowledge** | 3 | Independently able to write programs to strengthen the concepts covered in theory |
| 2 | Independently able to write programs but not able to strengthen the concepts learned in theory |
| 1 | Not able to write programs and not able to strengthen the concepts learned in theory |
| 8 | **Understanding of Engineering core** | 3 | Student uses appropriate methods, techniques to model and solve the problem accurately in the context of multidisciplinary projects  |
| 2 | Student tries to model the problem but fails to solve the problem in the context of multidisciplinary projects |
| 1 | Student fails to model the problem and also fails to solve the problem in the context of multidisciplinary projects |

**CSP Rubric Name & Number**

**Indirect Course Assessment Sheet**

**Tools:**

1. **Case Study**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.No.** | **Hall Ticket Number** | **Rubric Assessment** | **Remarks** |
| 1 |  |  |  |
| 2 |  |  |  |
| 3 |  |  |  |

1. **Course End Survey Report**

**Add-on Programmes (Guest Lecture/Video Lecture/Poster Presentation):**

1. Guest lecture is planned on CPU Organization (Before mid sem 1)
2. Guest lecture is planned on I/O Interface (After mid sem 1)

**Unit Wise PPT’s & Lecture Notes**