ANURAG GROUP OF INSTITUTIONS

(FORMERLY CVSR COLLEGE OF ENGINNERING)

Venkatapur (V), Ghatkesar (M), R.R.Dist.

ACTIVITY REPORT

Name of the activity**: Workshop**

Title /Topic **:" Advanced VLSI Design using Verilog HDL with Xilinx Vivado"**

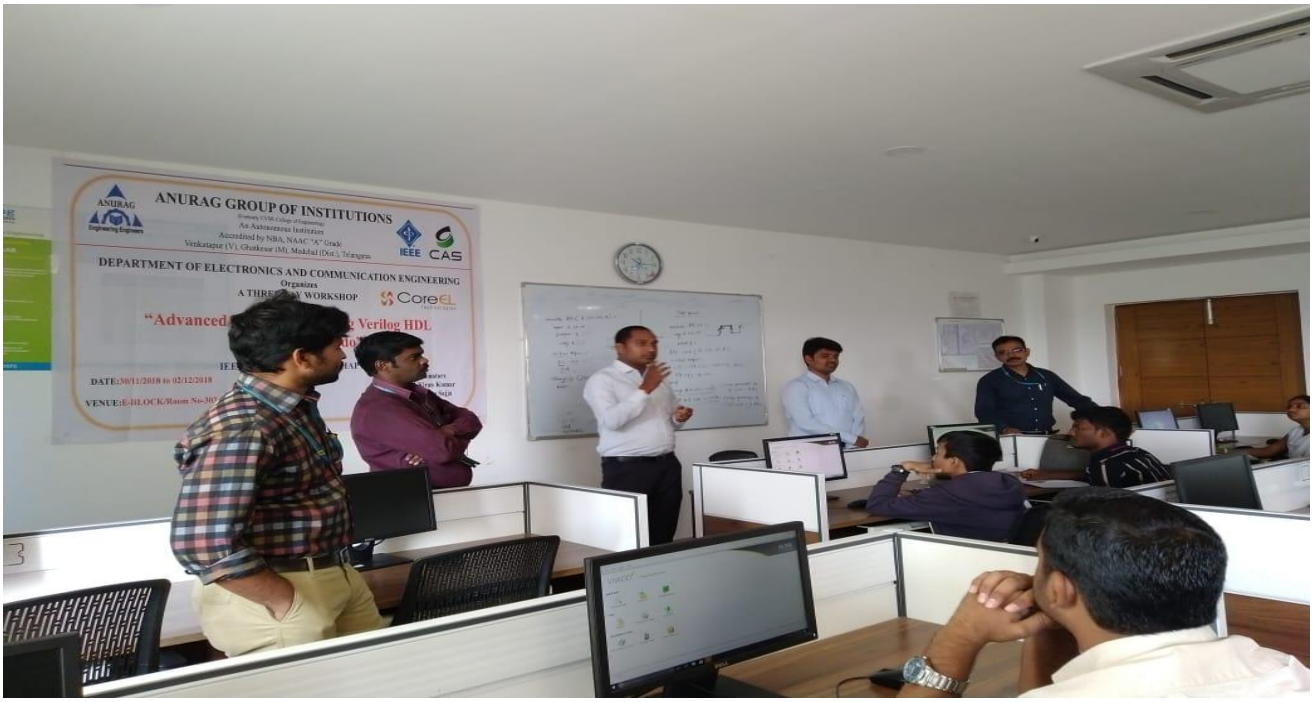
Resource Person: Mr.Nagender, **coreel and Applyvolt.**.

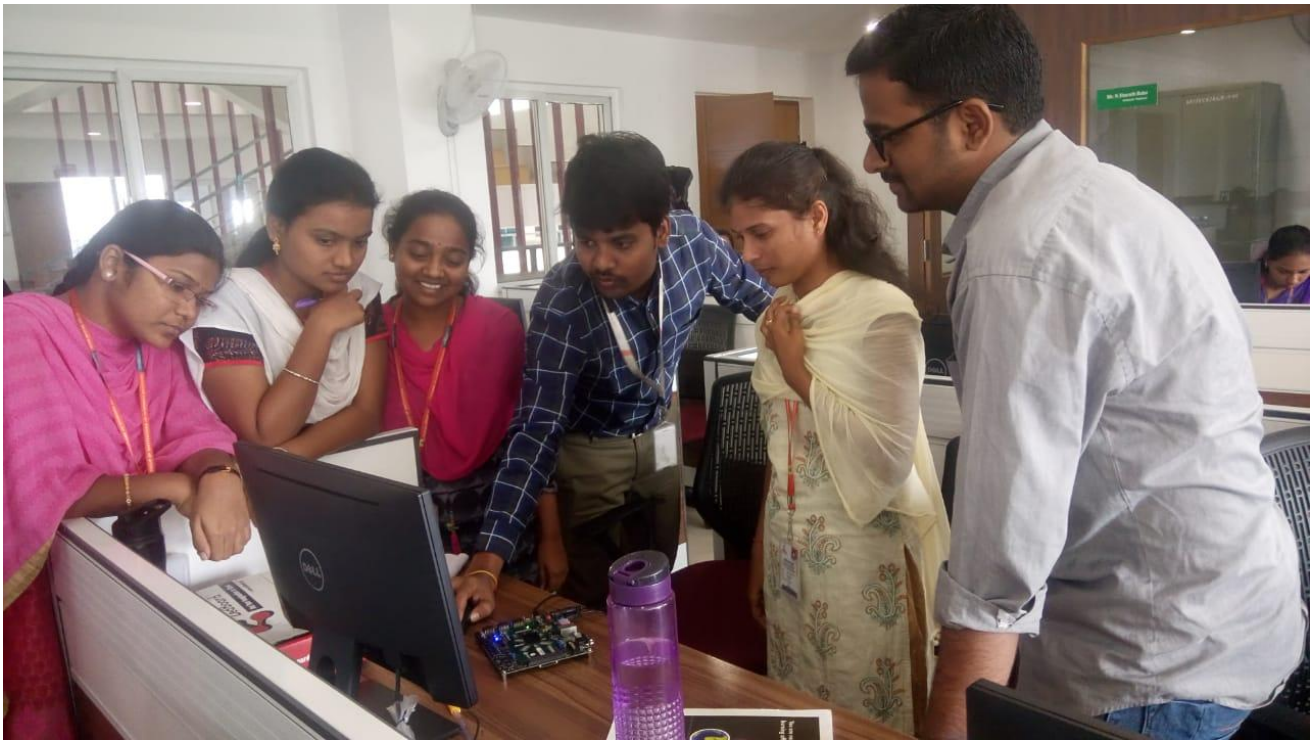
Date: **30/11/2018 to 02/12/2018.**

Key points: Interfacing, PMODs, Xilinx vivado.

Summary :Three day workshop on **Advanced VLSI Design using Verilog HDL with Xilinx Vivado**. III year ECE 24 students participated in the workshop, conducted in E- Block 303 LAB. The faculty co-ordinators are Mrs Amrita Sajja and Mr.Kiran kumar.

Photographs:





“Advanced VLSI Design using Verilog HDL with Xilinx Vivado”

30/11/2018 to 02/12/201

Report prepared by: Amrita sajja