ANURAG GROUP OF INSTITUTIONS

(FORMERLY CVSR COLLEGE OF ENGINNERING)
Venkatapur (V), Ghatkesar (M), Medchal Dist.

ACTIVITY REPORT

Name of the activity**: Guest lecture**

Title /Topic: **"IC DEVELOPMENT STAGES AND DESIGN CHALLENGES"**

Resource Person: **Mr. C.S Basha**, Manager; **Mr.R.Anil Kumar**, Design Engineer,

SION Semiconductors Pvt. Ltd.

Date: 27-03-2019

Key points: VLSI design, RTL design and Backend Design.

Summary: One day guest lecture on basics of VLSI design methodology, VHDL vs Verilog, HDL with examples, Product Planning, Advanced Design Flow, ASSP, ASIC AND Backend Design. III year B.Tech , IV year B.Tech ECE & M.Tech students are participated in E- Block Auditorium.

Photographs:

ANURAG GROUP OF INSTITUTIONS
(Formely CVSR College Of Engineering)
An Autonomous Institution
NBA & NAAC "A" Accreditation ,Approved By AICTE
Venkatapur(V),Ghatkesar(M),Medchal(Dist),Telangana State

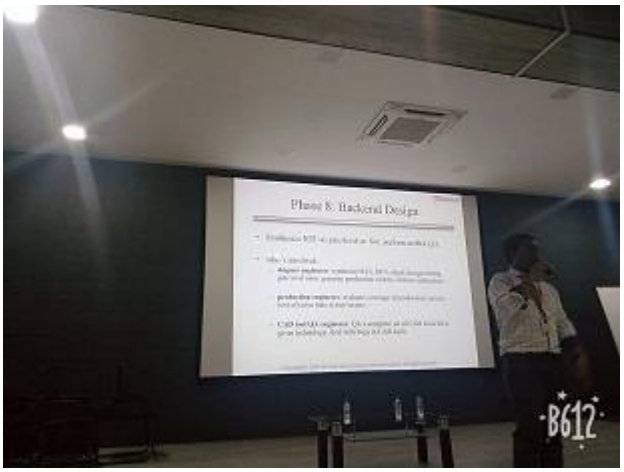
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

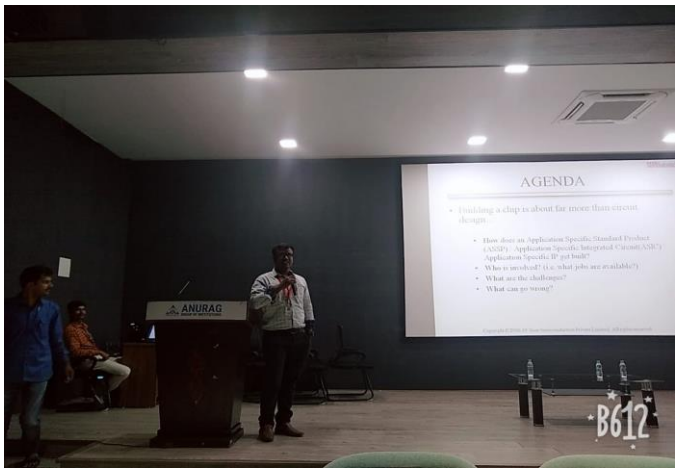
Guest Lecture On
"IC DEVELOPMENT STAGES AND DESIGN CHALLENGES"
In Association With IEI AGI ECSC Chapter
On 27 -03-2019
By

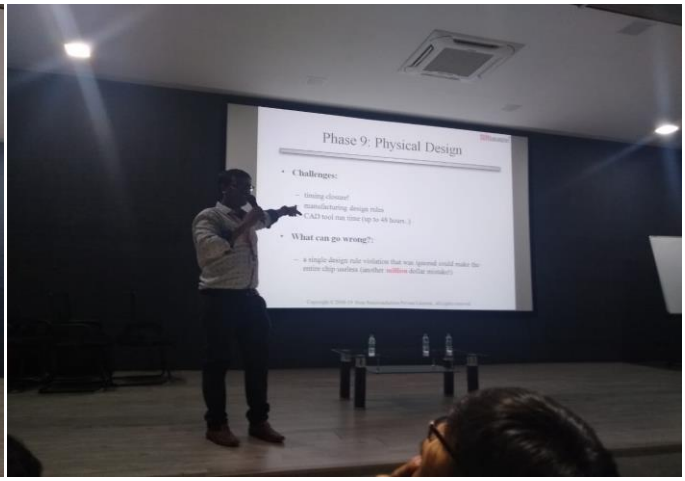
Mr.R.Anil Kumar
FPGA RTL Design Engineer
Sion Semiconductors Pvt.Ltd.

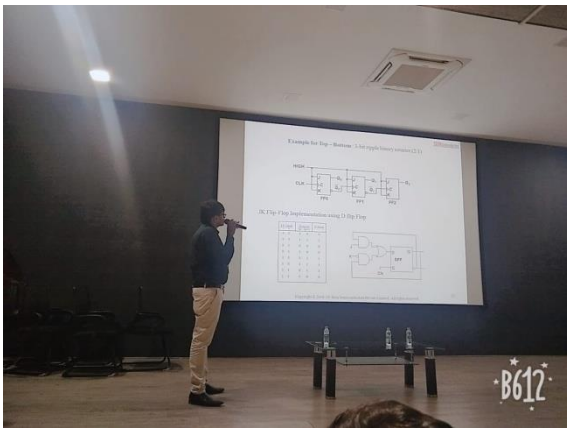
Program Co-ordinators:
1.Mrs.T.Annamani
2.Mr.E.Srinivas

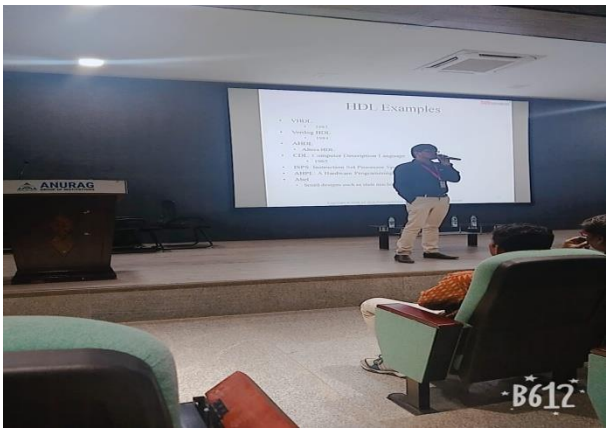
Venue:
E-Block
Auditorium











Report prepared by**: Mrs.T.Annamani** **HOD/ECE**